REMARKS

Claims 54-70 have been added. Claims 41 and 43-70 are pending in the application. Reconsideration is requested in view of the amendments and the remarks to follow.

Claims 41, 45, 46 and 50 stand rejected under 35 U.S.C. §102(b) as being anticipated by Kurimoto, U.S. Patent No. 5,306,655. Claims 41, 45, 46 and 50 stand rejected under 35 U.S.C. §102(b) as being anticipated by, or under 35 U.S.C. §103(a) as being unpatentable over, Verhaar, U.S. Patent No. 5,015,598, with Hiroki et al., U.S. Patent No. 5,512,771 as evidence. Claims 43 and 47 stand rejected under U.S.C. §103(a) as being unpatentable over Verhaar/Hiroki et al. or Kurimoto, in view of Pintchovski et al., U.S. Patent No. 5,126,283. Claims 44, 48, 49 and 51-53 stand rejected under U.S.C. §103(a) as being unpatentable over Verhaar/Hiroki et al. or Kurimoto, in view of Pintchovski et al., and further of Brigham et al., U.S. Patent No. 5,714,413, and Kumagai et al., U.S. Patent No. 5,430,313.

Anticipation is a legal term of art. Applicant notes that in order to provide a valid finding of anticipation, several conditions must be met: (i) the reference must include every element of the claim within the four corners of the reference (see MPEP §2121); (ii) the elements must be set forth as they are recited in the claim (see MPEP §2131); (iii) the teachings of the reference cannot be modified (see MPEP §706.02, stating that "No question of obviousness is present" in conjunction with anticipation); and (iv) the reference must enable the invention as recited

in the claim (see MPEP §2121.01). Additionally, (v) these conditions must be simultaneously satisfied.

Claim 41 recites "forming a conductive gate electrode over a gate dielectric layer on a substrate, the gate electrode having sidewalls and an interface with the gate dielectric layer; forming sidewall spacers comprising nitride on the gate electrode's sidewalls", which is not taught or disclosed by Kurimoto. Kurimoto does not teach formation of sidewall spacers on the sidewalls of a conductive gate electrode and instead teaches formation of sidewall spacers on a dielectric formed on sidewalls of a conductive gate electrode.

Claim 45 recites "forming a conductive gate structure on a first layer which is disposed on a substrate, the gate structure comprising a gate electrode having sidewalls and an interface with the first layer; forming sidewall spacers laterally adjacent the conductive gate structure's sidewalls sufficiently to cover all conductive material comprising the sidewalls, the sidewall spacers comprising an oxidation resistant material", which is not taught or disclosed by Kurimoto.

Applicant is using the term "laterally adjacent" to mean "having a common border", in conformance with a definition found on page 14 in Merriam-Webster's Collegiate Dictionary, Tenth Ed. (Merriam-Webster, Inc., Springfield, MA, principal copyright 1993; copy enclosed herewith). This is also in conformance with Applicant's drawings (see Fig. 8) and specification.

Claim 50 recites "forming a conductive gate structure over the dielectric layer, the gate structure having sidewalls defining a lateral dimension of the gate structure; forming non-oxide material over the gate structure and the dielectric layer; anisotropically etching the non-oxide material to form spacers on the sidewalls", which is not taught or disclosed by Kurimoto. The sidewall spacers taught by Kurimoto are not formed on sidewalls that define a lateral dimension of the gate structure, rather, Kurimoto's sidewalls are formed spaced apart from the gate structure by an intervening oxide layer.

Accordingly, the anticipation rejections based on Kurimoto are in error and should be withdrawn, and claims 41, 45, 46 and 50 should be allowed.

Claim 41 recites "after forming the sidewall spacers comprising nitride, exposing the substrate to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers joined therewith, wherein a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric layer, is oxidized", which is not taught, disclosed, suggested or motivated by the cited references, alone or in any proper combination. Claims 45 and 50 also include recitation of oxidation of a portion of the gate.

Verhaar teaches a process whereby a portion of the substrate 10 is oxidized or "regenerated" to form a gate dielectric 11 (see, e.g., Figs. 5-10; text at col. 5, lines 45-52). Verhaar is void of any teaching of oxidizing gate material. In fact, Verhaar explicitly teaches that oxidation

is limited to parts of the device "which are not protected by the provisional spacers 20a." (col. 5, lines 28-39). Verhaar teaches optional removal of exposed oxide (col. 3, lines 27-30). Verhaar further teaches (col. 3, lines 31-34) reoxidation and "regeneration" being effected "in the lateral direction over a short distance under the spacers" and does not provide any teaching, disclosure, suggestion or motivation to oxidize gate material.

As a result, Verhaar fails to anticipate the invention as recited in the claims (see MPEP §2131). As another result, Verhaar also fails to provide all of the elements recited in the claims, as is required for a finding of unpatentability (see MPEP §706.02(j)).

Verhaar additionally teaches careful control of the gate edges relative to various portions of the source and drain implants (see Field of the Invention, Background, Summary, Description). Verhaar further teaches that control of oxide thicknesses and gate conductivity are crucial (col. 2, lines 8-17). Accordingly, Verhaar teaches away from the modifications proposed by the Examiner for multiple reasons (see MPEP §2141.02 and §2145(X)(D)(2)).

Verhaar does not teach oxidation of the gate. There is simply no such teaching contained in Verhaar. Verhaar teaches (col. 5, lines 28-32) that "As a result of the operation of etching the first polycrystalline layer 12 and the ion implantation 21, the ends of the insulating gate layer 11 at the edges of the gate islands 15 and especially under the provisional spacers 20a have become degraded and/or polluted. In order to ensure a

satisfactory operation of the device of the MIS type, it is therefore necessary to regenerate the parts of the insulating gate layer 11 in the proximity of these ends situated under the provisional spacers 20a, which is attained, as indicated in FIG. 5, by a step of reoxidation of the parts of the device which are not protected by the provisional spacers 20a."

Such does not teach or disclose oxidation of the gate electrode material. The Examiner contends that such is inherent, and also contends that the burden is shifted to Applicant to demonstrate otherwise. The Examiner is mistaken on multiple grounds.

As noted above, Verhaar teaches "regeneration" of oxide on parts of the device which are not protected by the provisional spacers 20a". Verhaar explicitly teaches (col. 5, lines 4-9) that "Subsequently, the major part of the protective silicon nitride layer 20 is etched by an anisotropic etching method, for example reactive fluorine or chlorine ion etching, so as to form provisional narrow spacers 20a for the protection of the edges of the gate islands 15, as is indicated in FIG. 4."

Verhaar clearly is teaching a method for avoiding the result that is the proposition that the Examiner is citing Verhaar for. Accordingly, Verhaar does not teach or disclose the invention as recited in any of Applicant's claims 41, 45, 50, 52 and 53, all of which recite oxidation of a portion of the gate electrode material.

Applicant notes the requirements of MPEP §2143.01, entitled "Suggestion or Motivation To Modify the References", stating that: "THE PRIOR ART MUST SUGGEST THE DESIRABILITY OF THE CLAIMED

INVENTION". This MPEP section further states that "There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998) (The combination of the references taught every element of the claimed invention, however without a motivation to combine, a rejection based on a prima facie case of obvious was held improper.). The level of skill in the art cannot be relied upon to provide the suggestion to combine references. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999)."

In a subsection entitled "FACT THAT REFERENCES CAN BE COMBINED OR MODIFIED IS NOT SUFFICIENT TO ESTABLISH PRIMA FACIE OBVIOUSNESS", this MPEP section further states that: "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)."

Furthermore, Verhaar clearly teaches away from anything that would result in a "smiling gate". Given the lengths that Verhaar goes to in order to avoid what the Examiner is labeling an "inherent" result, the teachings of Verhaar are rendered unsuitable for their intended purpose by the modifications proposed by the Examiner. It is improper to apply the teachings of a reference in a manner that renders them unsuitable for their intended purpose. This is explained below in more detail.

Applicant notes the requirements of MPEP §2143.01, in a subsection entitled "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE". This subsection further states that "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)". Verhaar clearly states that the intended purpose of the nitride sidewalls is to prevent oxidation of the gate sidewalls.

The Examiner offers an inherency argument, citing In re King, 231 USPQ 136. King deals with an application directed to a method of optical interference that was anticipated by an article of manufacture. In King, the article of manufacture described in the prior art of Donley, U.S. Patent No. 3,9878,272, necessarily had to function in accordance with the method.

In other words, it was incapable of functioning any other way. "Under the principles of inherency, if a structure in the prior art necessarily functions in accordance with the limitations of a process or method claim of an application, the claim is anticipated."

King attempted to claim physical principles of partial reflection and constructive and destructive interference. As a result, the apparatus cited as anticipating these physical principles could not do anything but what King attempted to claim.

In the instant situation, significant changes in degree of oxidation are possible with variations in numerous parameters, such as: (i) temperature, (ii) oxide thickness, (iii) manner in which the gate dielectric was formed, (iv) oxidation time and a plethora of other variables. As a result, the structure and method taught by Verhaar does not necessarily function in accordance with Applicant's claim. The Examiner is confusing inherency with possibility. In this case, Verhaar explicitly teaches controlling the processing parameters to limit what is and what is not oxidized.

In fact, semiconductor manufacturing is notorious for being sufficiently sensitive to relatively small perturbations in conditions to such an extent that such manufacturers rigorously control processing parameters. Additionally, such manufacturers vigorously test the processes as well as parts being manufactured to determine when deviations crop up and to remediate such effects immediately. Oxidation rates for silicon depend on numerous variables, including dopant concentration, crystallinity and/or phase and other variables. As a result, all semiconductor device manufacturing involves experimental determination of processing conditions and parameters, relative concentrations and the like to achieve a desired result.

Verhaar clearly shows that the result of "tweaking" Verhaar's process does not involve oxidation of gate material, and Verhaar stresses the importance of maintaining appropriate gate geometry. In fact, such

reasons are Verhaar's *raison d'etre* (see, e.g., Field of the Invention, Background, Summary, Description).

Accordingly, the Examiner is mistaken in asserting that the burden is shifted to Applicant to prove that inherency does not exist, and, to the extent that any such burden might fall on Applicant, Applicant has successfully rebutted same. Additionally, the Examiner has failed to adequately respond to this rebuttal.

Further, Verhaar explicitly teaches (see col. 5, lines 4-9 and 28-32) controlling these process variables in such a manner to limit oxidation to the area beneath the sidewalls and is careful to show exactly and only this in Figs. 5-10. In other words, Verhaar show the gate electrode edges to comprise right angle corners in all of Figs. 2 through 10.

There is no text whatsoever in Verhaar to support the Examiner's contention that Verhaar is forming a "smiling gate" and there is text showing that Verhaar has adopted process techniques explicitly intended to avoid such. The Examiner states (p. 7) that nowhere does Verhaar show forming the device showing "exactly and only" this in Figs. 5-10. What the Examiner fails to note is that (i) Verhaar does show this and (ii) does not show or suggest anything else.

As noted above, Verhaar explicitly teaches away from oxidation of the gate material. Accordingly, all of the rejections based on Verhaar are prima facie defective and should be withdrawn, and claims 41 and 43-53 should be allowed.

Hiroki et al. teach formation of an oxide layer 6 adjacent a gate structure 5b. In contrast, Applicants recite "forming sidewall spacers comprising nitride on the gate electrode's sidewalls, the sidewall spacers joining with the gate dielectric layer" (claim 41); "forming sidewall spacers laterally adjacent the conductive gate structure's sidewalls sufficiently to cover all conductive material comprising the sidewalls, the sidewall spacers comprising an oxidation resistant material" (claim 45); "forming non-oxide material over the gate structure and the dielectric layer" (claim 50); and "covering a top and sidewalls of the gate structure with an oxidation resistant material" (claim 52); and "covering a top and sidewalls of the gate structure with an oxidation resistant material" (claim 53).

It is abundantly clear that Hiroki et al. do not teach, disclose, suggest or motivate the invention as recited in any of these claims. This is clear because Hiroki et al. explicitly teach formation of an oxide adjacent the gate material and do so in order to facilitate oxidation of the gate. In other words, Hiroki et al. require a material that (i) is an oxide and (ii) is not oxidation resistant. As a result, it is inconceivable that Hiroki et al. could teach, disclose, suggest or motivate the invention as recited in any of Applicant's claims.

Pintchovski et al. teach a process whereby an Al_2O_3 layer is employed to encapsulate a refractory metal conductor (see, e.g., Abstract). Pintchovski et al. do this in order to optimize conductivity of the conductor by permitting use of pure metal, rather than a silicide or semiconductor materials.

In fact, Pintchovski et al. explicitly teach (col. 1, lines 26-29) that prevention of oxidation of the conductors is a problem to be solved. Pintchovski et al. also explicitly teach (col. 2, lines 38-41) that the layer inhibits such oxidation. As such, Pintchovski et al. clearly teach away from the invention as recited in any of Applicant's claims.

Not only do Pintchovski et al. explicitly teach away from the invention as recited in any of Applicant's claims, but the intended purpose of Pintchovski et al. is destroyed in attempting to modify the teachings of Pintchovski et al. to try to arrive at the subject matter of Applicant's claims (see MPEP §2143.01). As a result, there is no motivation, as a matter of law, to attempt to employ the teachings of Pintchovski et al. in rejecting any of Applicant's claims.

Brigham et al. explicitly teach (Figs 2a-2c and 3a-3d) formation of "reox" oxide layer 24 or 34, completely surrounding the gate electrode. Further, Brigham et al. teach (Background; cols. 3-9) that the "reox" layer is critical to formation of high performance transistors.

As a result, not only do Brigham et al. explicitly teach away from the invention as recited in any of Applicant's claims, but the intended purpose of Brigham et al. is destroyed in attempting to modify the teachings of Brigham et al. to try to arrive at the subject matter of Applicant's claims. As a result, there is no motivation, as a matter of law (see MPEP §2143.01), to attempt to employ the teachings of Brigham et al. in rejecting any of Applicant's claims.

Kumagai et al. teach (Background) that short channel LDD MOSFETs have difficulty forming inversion regions rapidly and thus are limited in current carrying capability and are difficult to provide adequate drive signals to. As a result, Kumagai et al. teach (Abstract; Summary; embodiments described in Detailed Description) the benefits of using a sidewall spacer immediately adjacent the gate electrode that has a higher dielectric constant than the gate. This configuration concentrates electrical flux into an area where the transistors taught by Kumagai et al. benefit therefrom.

This benefit is completely destroyed in adapting the teachings of Kumagai et al. to try to arrive at the invention as recited in any of Applicant's claims because the dielectric constant resulting from oxidation of Kumagai et al.'s polysilicon gate material 12 is much lower than that of the high dielectric constant sidewall structures taught by Kumagai et al. and in fact is comparable to the dielectric constant of the gate dielectric taught by Kumagai et al. Accordingly, there is no motivation, as a matter of law, to attempt to modify the teachings of Kumagai et al. to try to arrive at the subject matter of any of Applicant's claims.

Claims 43, 44, 46-49 and 51 variously depend from Applicant's independent claims. As a result, these claims incorporate the recitation of the associated independent claims by reference (35 U.S.C. 112, 4TH ¶) As noted above with respect to Hiroki et al., none of these claims are compatible with these teachings.

For at least these reasons, the rejections of all of Applicant's claims are prima facie defective and should be withdrawn, and claims 41 and 43-53 should be allowed.

New claims 54-70 are supported at least by text appearing at p. 4, line 5 through p. 11, line 5 of the specification as originally filed. No new matter is added by new claims 54-70 (see MPEP §2163.06). New claims 54-70 distinguish over the art of record and are allowable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**".

The Examiner's response to argument is deficient in multiple regards. A first deficiency is that the response to argument clearly fails to respond to Applicant's arguments with respect to the rejections under 35 U.S.C. §102, or, in the alternative, is an admission that these rejections are defective.

Applicants note the requirements of MPEP §707.07, entitled "Completeness and Clarity of Examiner's Action". This MPEP section cites 37 CFR §1.104, entitled "Nature of examination" which in turn states, in subsection (b), entitled "Completeness of examiner's action" that "The examiner's action will be complete as to all matters, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters before further action is made."

This MPEP section further states, under a heading labeled "Examiner Note" that "The Examiner must, however, address any arguments presented by the applicant which are still relevant to any references being applied." The Office Action clearly fails to comport with these requirements as set forth in the MPEP, at least because the Office Action both fails to address Applicant's arguments with respect to anticipation and continues to reject claims as being anticipated over the same references. For example, Applicant has demonstrated that the law requires that the reference show all of the features recited in the claim, that the features must be arranged as they are set forth in the claim and that the reference must enable the invention as recited in the claim. The Examiner has failed to show that the references meet these standards.

A second deficiency is that the even under the unpatentability rejections, the combinations fail to provide all of the features recited in any of Applicant's independent claims. Applicants have reviewed the cited references and find that the allegations of claimed features being found in the references are clearly and plainly inaccurate.

A third deficiency is the failure to respond to Applicant's legal arguments regarding patentability of Applicant's claims. Simply ignoring these and merely repeating that "it would be obvious" to provide the features recited in the claims does not constitute a basis for rejection of the claims, particularly when the references fail to provide the features recited in the claims and the rejections fail to meet the standards for such rejections as set forth in the MPEP and as demonstrated by Applicant.

For example, Applicant has demonstrated that the arguments to the effect that the burden of showing "inherency" with respect to Verhaar's teachings are inapposite. The Examiner has not responded to these arguments, which are repeated above. Applicant has shown that the references teach away from the invention as recited in the claims and/or are rendered unsuitable for their intended purposes. The Examiner has not provided meaningful rebuttal of these arguments.

For at least these reasons, the Office Action fails to comport with appropriate standards for examination. The Examiner should either allow Applicant's claims or provide a meaningful basis for rejection and an appropriate response to Applicant's arguments.

Applicant respectfully asserts that claims 41 and 43-70 are in condition for allowance. Action to that effect is earnestly sought. If, however the Examiner's next action is anything other than a Notice of Allowance, the Examiner is requested to call the undersigned to schedule a telephonic interview. The undersigned is available during normal business hours, Pacific Coast Time.

Respectfully submitted,

Dated: Aug. 8, 2002 By: _____

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Version with markings to show changes made.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/059,644
Filing Date ..... April 13, 1998
Inventor ..... Pai-Hung Pan
Assignee ..... Micron Technology, Inc.
Group Art Unit 2822
Examiner ..... M. Trinh
Attorney's Docket No. MI22-898
Title: Semiconductor Processing Methods of Forming a Conductive Gate and Line

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY RESPONSE TO MAY 8, 2002 OFFICE ACTION

Underlines indicate insertions and brackets indicate deletions.

New claims 53-70 have been added.

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